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; Filename keiltest.asm

; Project keiltest.DAV

;----------------------------------------------------------------------------

; Description This file contains the assembler formatted information

; about the actual project values. It will be used by your

; programming environment.

;

; PLEASE DO NOT MODIFY THIS FILE !

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;----------------------------------------------------------------------------

; Date 10.02.2005 10:10:14

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;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

; RMAP=0 PAGE=1 - ADC Channel 0 Control Register

ADC\_CHCTR0\_LCC SET 0

ADC\_CHCTR0\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 1 Control Register

ADC\_CHCTR1\_LCC SET 0

ADC\_CHCTR1\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 2 Control Register

ADC\_CHCTR2\_LCC SET 0

ADC\_CHCTR2\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 3 Control Register

ADC\_CHCTR3\_LCC SET 0

ADC\_CHCTR3\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 4 Control Register

ADC\_CHCTR4\_LCC SET 0

ADC\_CHCTR4\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 5 Control Register

ADC\_CHCTR5\_LCC SET 0

ADC\_CHCTR5\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 6 Control Register

ADC\_CHCTR6\_LCC SET 0

ADC\_CHCTR6\_RESRSEL SET 0

; RMAP=0 PAGE=1 - ADC Channel 7 Control Register

ADC\_CHCTR7\_LCC SET 0

ADC\_CHCTR7\_RESRSEL SET 0

; RMAP=0 PAGE=5 - ADC Channel Interrupt Clear Register

ADC\_CHINCR\_CHINC0 SET 0

ADC\_CHINCR\_CHINC1 SET 0

ADC\_CHINCR\_CHINC2 SET 0

ADC\_CHINCR\_CHINC3 SET 0

ADC\_CHINCR\_CHINC4 SET 0

ADC\_CHINCR\_CHINC5 SET 0

ADC\_CHINCR\_CHINC6 SET 0

ADC\_CHINCR\_CHINC7 SET 0

; RMAP=0 PAGE=5 - ADC Channel Interrupt Flag Register

ADC\_CHINFR\_CHINF0 SET 0

ADC\_CHINFR\_CHINF1 SET 0

ADC\_CHINFR\_CHINF2 SET 0

ADC\_CHINFR\_CHINF3 SET 0

ADC\_CHINFR\_CHINF4 SET 0

ADC\_CHINFR\_CHINF5 SET 0

ADC\_CHINFR\_CHINF6 SET 0

ADC\_CHINFR\_CHINF7 SET 0

; RMAP=0 PAGE=5 - ADC Channel Interrupt Node Pointer Register

ADC\_CHINPR\_CHINP0 SET 0

ADC\_CHINPR\_CHINP1 SET 0

ADC\_CHINPR\_CHINP2 SET 0

ADC\_CHINPR\_CHINP3 SET 0

ADC\_CHINPR\_CHINP4 SET 0

ADC\_CHINPR\_CHINP5 SET 0

ADC\_CHINPR\_CHINP6 SET 0

ADC\_CHINPR\_CHINP7 SET 0

; RMAP=0 PAGE=5 - ADC Channel Interrupt Set Register

ADC\_CHINSR\_CHINS0 SET 0

ADC\_CHINSR\_CHINS1 SET 0

ADC\_CHINSR\_CHINS2 SET 0

ADC\_CHINSR\_CHINS3 SET 0

ADC\_CHINSR\_CHINS4 SET 0

ADC\_CHINSR\_CHINS5 SET 0

ADC\_CHINSR\_CHINS6 SET 0

ADC\_CHINSR\_CHINS7 SET 0

; RMAP=0 PAGE=6 - ADC Source 1 Conversion Request Control Register

ADC\_CRCR1\_CH4 SET 0

ADC\_CRCR1\_CH5 SET 0

ADC\_CRCR1\_CH6 SET 0

ADC\_CRCR1\_CH7 SET 0

; RMAP=0 PAGE=6 - ADC Source 1 Conversion Request Mode Register

ADC\_CRMR1\_CLRPND SET 0

ADC\_CRMR1\_ENGT SET 0

ADC\_CRMR1\_ENSI SET 0

ADC\_CRMR1\_ENTR SET 0

ADC\_CRMR1\_LDEV SET 0

ADC\_CRMR1\_SCAN SET 0

; RMAP=0 PAGE=6 - ADC Source 1 Conversion Request Pending Register

ADC\_CRPR1\_CHP4 SET 0

ADC\_CRPR1\_CHP5 SET 0

ADC\_CRPR1\_CHP6 SET 0

ADC\_CRPR1\_CHP7 SET 0

; RMAP=0 PAGE=0 - ADC External Trigger Control Register

ADC\_ETRCR\_ETRSEL0 SET 0

ADC\_ETRCR\_ETRSEL1 SET 0

ADC\_ETRCR\_SYNEN0 SET 0

ADC\_ETRCR\_SYNEN1 SET 0

; RMAP=0 PAGE=5 - ADC Event Interrupt Clear Register

ADC\_EVINCR\_EVINC0 SET 0

ADC\_EVINCR\_EVINC1 SET 0

ADC\_EVINCR\_EVINC4 SET 0

ADC\_EVINCR\_EVINC5 SET 0

ADC\_EVINCR\_EVINC6 SET 0

ADC\_EVINCR\_EVINC7 SET 0

; RMAP=0 PAGE=5 - ADC Event Interrupt Flag Register

ADC\_EVINFR\_EVINF0 SET 0

ADC\_EVINFR\_EVINF1 SET 0

ADC\_EVINFR\_EVINF4 SET 0

ADC\_EVINFR\_EVINF5 SET 0

ADC\_EVINFR\_EVINF6 SET 0

ADC\_EVINFR\_EVINF7 SET 0

; RMAP=0 PAGE=5 - ADC Event Interrupt Node Pointer Register

ADC\_EVINPR\_EVINP0 SET 0

ADC\_EVINPR\_EVINP1 SET 0

ADC\_EVINPR\_EVINP4 SET 0

ADC\_EVINPR\_EVINP5 SET 0

ADC\_EVINPR\_EVINP6 SET 0

ADC\_EVINPR\_EVINP7 SET 0

; RMAP=0 PAGE=5 - ADC Event Interrupt Set Flag Register

ADC\_EVINSR\_EVINS0 SET 0

ADC\_EVINSR\_EVINS1 SET 0

ADC\_EVINSR\_EVINS4 SET 0

ADC\_EVINSR\_EVINS5 SET 0

ADC\_EVINSR\_EVINS6 SET 0

ADC\_EVINSR\_EVINS7 SET 0

; RMAP=0 PAGE=0 - ADC Global Control Register

ADC\_GLOBCTR\_ANON SET 0

ADC\_GLOBCTR\_CTC SET 3

ADC\_GLOBCTR\_DW SET 0

; RMAP=0 PAGE=0 - ADC Global Status Register

ADC\_GLOBSTR\_BUSY SET 0

ADC\_GLOBSTR\_CHNR SET 0

ADC\_GLOBSTR\_SAMPLE SET 0

; RMAP=0 PAGE=0 - ADC Input Class 0 Register

ADC\_INPCR0\_STC SET 0

; RMAP=0 PAGE=0 - ADC Limit Check Boundary Register

ADC\_LCBR\_BOUND0 SET 7

ADC\_LCBR\_BOUND1 SET 11

; RMAP=0 - ADC Page Register

ADC\_PAGE\_OP SET 0

ADC\_PAGE\_PAGE SET 0

ADC\_PAGE\_STNR SET 0

; RMAP=0 PAGE=0 - ADC Priority and Arbitration Register

ADC\_PRAR\_ARBM SET 0

ADC\_PRAR\_ASEN0 SET 0

ADC\_PRAR\_ASEN1 SET 0

ADC\_PRAR\_CSM0 SET 0

ADC\_PRAR\_CSM1 SET 0

ADC\_PRAR\_PRIO0 SET 0

ADC\_PRAR\_PRIO1 SET 0

; RMAP=0 PAGE=6 - ADC Source 0 Queue 0 Register

ADC\_Q0R0\_ENSI SET 0

ADC\_Q0R0\_EXTR SET 0

ADC\_Q0R0\_REQCHNR SET 0

ADC\_Q0R0\_RF SET 0

ADC\_Q0R0\_V SET 0

; RMAP=0 PAGE=6 - ADC Source 0 Queue Backup Register

ADC\_QBUR0\_ENSI SET 0

ADC\_QBUR0\_EXTR SET 0

ADC\_QBUR0\_REQCHNR SET 0

ADC\_QBUR0\_RF SET 0

ADC\_QBUR0\_V SET 0

; RMAP=0 PAGE=6 - ADC Source 0 Queue Input Register

ADC\_QINR0\_ENSI SET 0

ADC\_QINR0\_EXTR SET 0

ADC\_QINR0\_REQCHNR SET 0

ADC\_QINR0\_RF SET 0

; RMAP=0 PAGE=6 - ADC Source 0 Queue Mode Register

ADC\_QMR0\_CEV SET 0

ADC\_QMR0\_CLRV SET 0

ADC\_QMR0\_ENGT SET 0

ADC\_QMR0\_ENTR SET 0

ADC\_QMR0\_FLUSH SET 0

ADC\_QMR0\_TREV SET 0

ADC\_QMR0\_TRMD SET 0

; RMAP=0 PAGE=6 - ADC Source 0 Queue Status Register

ADC\_QSR0\_EMPTY SET 0

ADC\_QSR0\_EV SET 0

; RMAP=0 PAGE=4 - ADC Result 0 Control Register

ADC\_RCR0\_DRCTR SET 0

ADC\_RCR0\_FEN SET 0

ADC\_RCR0\_IEN SET 0

ADC\_RCR0\_VFCTR SET 0

ADC\_RCR0\_WFR SET 0

; RMAP=0 PAGE=4 - ADC Result 1 Control Register

ADC\_RCR1\_DRCTR SET 0

ADC\_RCR1\_FEN SET 0

ADC\_RCR1\_IEN SET 0

ADC\_RCR1\_VFCTR SET 0

ADC\_RCR1\_WFR SET 0

; RMAP=0 PAGE=4 - ADC Result 2 Control Register

ADC\_RCR2\_DRCTR SET 0

ADC\_RCR2\_FEN SET 0

ADC\_RCR2\_IEN SET 0

ADC\_RCR2\_VFCTR SET 0

ADC\_RCR2\_WFR SET 0

; RMAP=0 PAGE=4 - ADC Result 3 Control Register

ADC\_RCR3\_DRCTR SET 0

ADC\_RCR3\_FEN SET 0

ADC\_RCR3\_IEN SET 0

ADC\_RCR3\_VFCTR SET 0

ADC\_RCR3\_WFR SET 0

; RMAP=0 PAGE=2 - ADC Result 0 Register High

ADC\_RESR0H\_RESULT[9:2] SET 0

; RMAP=0 PAGE=2 - ADC Result 0 Register Low

ADC\_RESR0L\_CHNR SET 0

ADC\_RESR0L\_DRC SET 0

ADC\_RESR0L\_RESULT[1:0] SET 0

ADC\_RESR0L\_VF SET 0

; RMAP=0 PAGE=2 - ADC Result 1 Register High

ADC\_RESR1H\_RESULT[9:2] SET 0

; RMAP=0 PAGE=2 - ADC Result 1 Register Low

ADC\_RESR1L\_CHNR SET 0

ADC\_RESR1L\_DRC SET 0

ADC\_RESR1L\_RESULT[1:0] SET 0

ADC\_RESR1L\_VF SET 0

; RMAP=0 PAGE=2 - ADC Result 2 Register High

ADC\_RESR2H\_RESULT[9:2] SET 0

; RMAP=0 PAGE=2 - ADC Result 2 Register Low

ADC\_RESR2L\_CHNR SET 0

ADC\_RESR2L\_DRC SET 0

ADC\_RESR2L\_RESULT[1:0] SET 0

ADC\_RESR2L\_VF SET 0

; RMAP=0 PAGE=2 - ADC Result 3 Register High

ADC\_RESR3H\_RESULT[9:2] SET 0

; RMAP=0 PAGE=2 - ADC Result 3 Register Low

ADC\_RESR3L\_CHNR SET 0

ADC\_RESR3L\_DRC SET 0

ADC\_RESR3L\_RESULT[1:0] SET 0

ADC\_RESR3L\_VF SET 0

; RMAP=0 PAGE=3 - ADC Result 0 View A Register High

ADC\_RESRA0H\_RESULT[10:3] SET 0

; RMAP=0 PAGE=3 - ADC Result 0 View A Register Low

ADC\_RESRA0L\_CHNR SET 0

ADC\_RESRA0L\_DRC SET 0

ADC\_RESRA0L\_RESULT[2:0] SET 0

ADC\_RESRA0L\_VF SET 0

; RMAP=0 PAGE=3 - ADC Result 1 View A Register High

ADC\_RESRA1H\_RESULT[10:3] SET 0

; RMAP=0 PAGE=3 - ADC Result 1 View A Register Low

ADC\_RESRA1L\_CHNR SET 0

ADC\_RESRA1L\_DRC SET 0

ADC\_RESRA1L\_RESULT[2:0] SET 0

ADC\_RESRA1L\_VF SET 0

; RMAP=0 PAGE=3 - ADC Result 2 View A Register High

ADC\_RESRA2H\_RESULT[10:3] SET 0

; RMAP=0 PAGE=3 - ADC Result 2 View A Register Low

ADC\_RESRA2L\_CHNR SET 0

ADC\_RESRA2L\_DRC SET 0

ADC\_RESRA2L\_RESULT[2:0] SET 0

ADC\_RESRA2L\_VF SET 0

; RMAP=0 PAGE=3 - ADC Result 3 View A Register High

ADC\_RESRA3H\_RESULT[10:3] SET 0

; RMAP=0 PAGE=3 - ADC Result 3 View A Register Low

ADC\_RESRA3L\_CHNR SET 0

ADC\_RESRA3L\_DRC SET 0

ADC\_RESRA3L\_RESULT[2:0] SET 0

ADC\_RESRA3L\_VF SET 0

; RMAP=0 PAGE=4 - ADC Valid Flag Clear Register

ADC\_VFCR\_VFC0 SET 0

ADC\_VFCR\_VFC1 SET 0

ADC\_VFCR\_VFC2 SET 0

ADC\_VFCR\_VFC3 SET 0

; RMAP=x - CPU Accumulator Register

A\_ACC0 SET 0

A\_ACC1 SET 0

A\_ACC2 SET 0

A\_ACC3 SET 0

A\_ACC4 SET 0

A\_ACC5 SET 0

A\_ACC6 SET 0

A\_ACC7 SET 0

; RMAP=0 PAGE=0 - SCU Baud Rate Control Register

BCON\_BGSEL SET 0

BCON\_BREN SET 0

BCON\_BRPRE SET 0

BCON\_R SET 1

BCON\_T2EXIS SET 0

; RMAP=0 PAGE=0 - SCU Baud Rate Timer/Reload Register

BG\_BR\_VALUE SET 173

; RMAP=x - CPU B Register

B\_B0 SET 0

B\_B1 SET 0

B\_B2 SET 0

B\_B3 SET 0

B\_B4 SET 0

B\_B5 SET 0

B\_B6 SET 0

B\_B7 SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC60 High

CCU6\_CC60RH\_CC60VH SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC60 Low

CCU6\_CC60RL\_CC60VL SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC60 High

CCU6\_CC60SRH\_CC60SH SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC60 Low

CCU6\_CC60SRL\_CC60SL SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC61 High

CCU6\_CC61RH\_CC61VH SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC61 Low

CCU6\_CC61RL\_CC61VL SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC61 High

CCU6\_CC61SRH\_CC61SH SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC61 Low

CCU6\_CC61SRL\_CC61SL SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC62 High

CCU6\_CC62RH\_CC62VH SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC62 Low

CCU6\_CC62RL\_CC62VL SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC62 High

CCU6\_CC62SRH\_CC62SH SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC62 Low

CCU6\_CC62SRL\_CC62SL SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC63 High

CCU6\_CC63RH\_CC63VH SET 0

; RMAP=0 PAGE=1 - CCU6 Capture/Compare Register for Channel CC63 Low

CCU6\_CC63RL\_CC63VL SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC63 High

CCU6\_CC63SRH\_CC63SH SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Shadow Register for Channel CC63 Low

CCU6\_CC63SRL\_CC63SL SET 0

; RMAP=0 PAGE=0 - CCU6 Compare State Modification Register High

CCU6\_CMPMODIFH\_MCC60R SET 0

CCU6\_CMPMODIFH\_MCC61R SET 0

CCU6\_CMPMODIFH\_MCC62R SET 0

CCU6\_CMPMODIFH\_MCC63R SET 0

; RMAP=0 PAGE=0 - CCU6 Compare State Modification Register Low

CCU6\_CMPMODIFL\_MCC60S SET 0

CCU6\_CMPMODIFL\_MCC61S SET 0

CCU6\_CMPMODIFL\_MCC62S SET 0

CCU6\_CMPMODIFL\_MCC63S SET 0

; RMAP=0 PAGE=3 - CCU6 Compare State Register High

CCU6\_CMPSTATH\_CC60PS SET 0

CCU6\_CMPSTATH\_CC61PS SET 0

CCU6\_CMPSTATH\_CC62PS SET 0

CCU6\_CMPSTATH\_COUT60PS SET 0

CCU6\_CMPSTATH\_COUT61PS SET 0

CCU6\_CMPSTATH\_COUT62PS SET 0

CCU6\_CMPSTATH\_COUT63PS SET 0

CCU6\_CMPSTATH\_T13IM SET 0

; RMAP=0 PAGE=3 - CCU6 Compare State Register Low

CCU6\_CMPSTATL\_CC60ST SET 0

CCU6\_CMPSTATL\_CC61ST SET 0

CCU6\_CMPSTATL\_CC62ST SET 0

CCU6\_CMPSTATL\_CC63ST SET 0

CCU6\_CMPSTATL\_CCPOS0 SET 0

CCU6\_CMPSTATL\_CCPOS1 SET 0

CCU6\_CMPSTATL\_CCPOS2 SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Enable Register High

CCU6\_IENH\_ENCHE SET 0

CCU6\_IENH\_ENIDLE SET 0

CCU6\_IENH\_ENSTR SET 0

CCU6\_IENH\_ENT13CM SET 0

CCU6\_IENH\_ENT13PM SET 0

CCU6\_IENH\_ENTRPF SET 0

CCU6\_IENH\_ENWHE SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Enable Register Low

CCU6\_IENL\_ENCC60F SET 0

CCU6\_IENL\_ENCC60R SET 0

CCU6\_IENL\_ENCC61F SET 0

CCU6\_IENL\_ENCC61R SET 0

CCU6\_IENL\_ENCC62F SET 0

CCU6\_IENL\_ENCC62R SET 0

CCU6\_IENL\_ENT12OM SET 0

CCU6\_IENL\_ENT12PM SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Node Pointer Register High

CCU6\_INPH\_INPERR SET 0

CCU6\_INPH\_INPT12 SET 0

CCU6\_INPH\_INPT13 SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Node Pointer Register Low

CCU6\_INPL\_INPCC60 SET 0

CCU6\_INPL\_INPCC61 SET 0

CCU6\_INPL\_INPCC62 SET 0

CCU6\_INPL\_INPCHE SET 0

; RMAP=0 PAGE=3 - CCU6 Capture/Compare Interrupt Status Register High

CCU6\_ISH\_CHE SET 0

CCU6\_ISH\_IDLE SET 0

CCU6\_ISH\_STR SET 0

CCU6\_ISH\_T13CM SET 0

CCU6\_ISH\_T13PM SET 0

CCU6\_ISH\_TRPF SET 0

CCU6\_ISH\_TRPS SET 0

CCU6\_ISH\_WHE SET 0

; RMAP=0 PAGE=3 - CCU6 Capture/Compare Interrupt Status Register Low

CCU6\_ISL\_ICC60F SET 0

CCU6\_ISL\_ICC60R SET 0

CCU6\_ISL\_ICC61F SET 0

CCU6\_ISL\_ICC61R SET 0

CCU6\_ISL\_ICC62F SET 0

CCU6\_ISL\_ICC62R SET 0

CCU6\_ISL\_T12OM SET 0

CCU6\_ISL\_T12PM SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Interrupt Status Reset Register High

CCU6\_ISRH\_RCHE SET 0

CCU6\_ISRH\_RIDLE SET 0

CCU6\_ISRH\_RSTR SET 0

CCU6\_ISRH\_RT13CM SET 0

CCU6\_ISRH\_RT13PM SET 0

CCU6\_ISRH\_RTRPF SET 0

CCU6\_ISRH\_RWHE SET 0

; RMAP=0 PAGE=0 - CCU6 Capture/Compare Interrupt Status Reset Register Low

CCU6\_ISRL\_RCC60F SET 0

CCU6\_ISRL\_RCC60R SET 0

CCU6\_ISRL\_RCC61F SET 0

CCU6\_ISRL\_RCC61R SET 0

CCU6\_ISRL\_RCC62F SET 0

CCU6\_ISRL\_RCC62R SET 0

CCU6\_ISRL\_RT12OM SET 0

CCU6\_ISRL\_RT12PM SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Status Set Register High

CCU6\_ISSH\_SCHE SET 0

CCU6\_ISSH\_SIDLE SET 0

CCU6\_ISSH\_SSTR SET 0

CCU6\_ISSH\_ST13CM SET 0

CCU6\_ISSH\_ST13PM SET 0

CCU6\_ISSH\_STRPF SET 0

CCU6\_ISSH\_SWHC SET 0

CCU6\_ISSH\_SWHE SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Interrupt Status Set Register Low

CCU6\_ISSL\_SCC60F SET 0

CCU6\_ISSL\_SCC60R SET 0

CCU6\_ISSL\_SCC61F SET 0

CCU6\_ISSL\_SCC61R SET 0

CCU6\_ISSL\_SCC62F SET 0

CCU6\_ISSL\_SCC62R SET 0

CCU6\_ISSL\_ST12OM SET 0

CCU6\_ISSL\_ST12PM SET 0

; RMAP=0 PAGE=2 - CCU6 Multi-Channel Mode Control Register

CCU6\_MCMCTR\_SWSEL SET 0

CCU6\_MCMCTR\_SWSYN SET 0

; RMAP=0 PAGE=3 - CCU6 Multi-Channel Mode Output Register High

CCU6\_MCMOUTH\_CURH SET 0

CCU6\_MCMOUTH\_EXPH SET 0

; RMAP=0 PAGE=3 - CCU6 Multi-Channel Mode Output Register Low

CCU6\_MCMOUTL\_MCMP SET 0

CCU6\_MCMOUTL\_R SET 0

; RMAP=0 PAGE=0 - CCU6 Multi-Channel Mode Output Shadow Register High

CCU6\_MCMOUTSH\_CURHS SET 0

CCU6\_MCMOUTSH\_EXPHS SET 0

CCU6\_MCMOUTSH\_STRHP SET 0

; RMAP=0 PAGE=0 - CCU6 Multi-Channel Mode Output Shadow Register Low

CCU6\_MCMOUTSL\_MCMPS SET 0

CCU6\_MCMOUTSL\_STRMCM SET 0

; RMAP=0 PAGE=2 - CCU6 Modulation Control Register High

CCU6\_MODCTRH\_ECT13O SET 0

CCU6\_MODCTRH\_T13MODEN SET 0

; RMAP=0 PAGE=2 - CCU6 Modulation Control Register Low

CCU6\_MODCTRL\_MCMEN SET 0

CCU6\_MODCTRL\_T12MODEN SET 0

; RMAP=0 - CCU6 Page Register

CCU6\_PAGE\_OP SET 0

CCU6\_PAGE\_PAGE SET 0

CCU6\_PAGE\_STNR SET 0

; RMAP=0 PAGE=3 - CCU6 Port Input Select 0 Register High

CCU6\_PISEL0H\_ISPOS0 SET 0

CCU6\_PISEL0H\_ISPOS1 SET 0

CCU6\_PISEL0H\_ISPOS2 SET 0

CCU6\_PISEL0H\_IST12HR SET 0

; RMAP=0 PAGE=3 - CCU6 Port Input Select 0 Register Low

CCU6\_PISEL0L\_ISCC60 SET 0

CCU6\_PISEL0L\_ISCC61 SET 0

CCU6\_PISEL0L\_ISCC62 SET 0

CCU6\_PISEL0L\_ISTRP SET 0

; RMAP=0 PAGE=3 - CCU6 Port Input Select 2 Register

CCU6\_PISEL2\_IST13HR SET 0

; RMAP=0 PAGE=2 - CCU6 Passive State Level Register

CCU6\_PSLR\_PSL SET 0

CCU6\_PSLR\_PSL63 SET 0

; RMAP=0 PAGE=1 - CCU6 Dead-Time Control Register for Timer T12 High

CCU6\_T12DTCH\_DTE0 SET 0

CCU6\_T12DTCH\_DTE1 SET 0

CCU6\_T12DTCH\_DTE2 SET 0

CCU6\_T12DTCH\_DTR0 SET 0

CCU6\_T12DTCH\_DTR1 SET 0

CCU6\_T12DTCH\_DTR2 SET 0

; RMAP=0 PAGE=1 - CCU6 Dead-Time Control Register for Timer T12 Low

CCU6\_T12DTCL\_DTM SET 1

; RMAP=0 PAGE=3 - CCU6 Timer T12 Counter Register High

CCU6\_T12H\_T12CVH SET 0

; RMAP=0 PAGE=3 - CCU6 Timer T12 Counter Register Low

CCU6\_T12L\_T12CVL SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Mode Select Register High

CCU6\_T12MSELH\_DBYP SET 0

CCU6\_T12MSELH\_HSYNC SET 0

CCU6\_T12MSELH\_MSEL62 SET 0

; RMAP=0 PAGE=2 - CCU6 Capture/Compare Mode Select Register Low

CCU6\_T12MSELL\_MSEL60 SET 0

CCU6\_T12MSELL\_MSEL61 SET 0

; RMAP=0 PAGE=1 - CCU6 Timer T12 Period Register High

CCU6\_T12PRH\_T12PVH SET 0

; RMAP=0 PAGE=1 - CCU6 Timer T12 Period Register Low

CCU6\_T12PRL\_T12PVL SET 1

; RMAP=0 PAGE=3 - CCU6 Timer T13 Counter Register High

CCU6\_T13H\_T13CVH SET 0

; RMAP=0 PAGE=3 - CCU6 Timer T13 Counter Register Low

CCU6\_T13L\_T13CVL SET 0

; RMAP=0 PAGE=1 - CCU6 Timer T13 Period Register High

CCU6\_T13PRH\_T13PVH SET 0

; RMAP=0 PAGE=1 - CCU6 Timer T13 Period Register Low

CCU6\_T13PRL\_T13PVL SET 1

; RMAP=0 PAGE=1 - CCU6 Timer Control 0 Register High

CCU6\_TCTR0H\_STE13 SET 0

CCU6\_TCTR0H\_T13CLK SET 0

CCU6\_TCTR0H\_T13PRE SET 0

CCU6\_TCTR0H\_T13R SET 0

; RMAP=0 PAGE=1 - CCU6 Timer Control 0 Register Low

CCU6\_TCTR0L\_CDIR SET 0

CCU6\_TCTR0L\_CTM SET 0

CCU6\_TCTR0L\_STE12 SET 0

CCU6\_TCTR0L\_T12CLK SET 0

CCU6\_TCTR0L\_T12PRE SET 0

CCU6\_TCTR0L\_T12R SET 0

; RMAP=0 PAGE=2 - CCU6 Timer Control 2 Register High

CCU6\_TCTR2H\_T12RSEL SET 0

CCU6\_TCTR2H\_T13RSEL SET 0

; RMAP=0 PAGE=2 - CCU6 Timer Control 2 Register Low

CCU6\_TCTR2L\_T12SSC SET 0

CCU6\_TCTR2L\_T13SSC SET 0

CCU6\_TCTR2L\_T13TEC SET 0

CCU6\_TCTR2L\_T13TED SET 1

; RMAP=0 PAGE=0 - CCU6 Timer Control 4 Register High

CCU6\_TCTR4H\_T13RES SET 0

CCU6\_TCTR4H\_T13RR SET 0

CCU6\_TCTR4H\_T13RS SET 0

CCU6\_TCTR4H\_T13STD SET 0

CCU6\_TCTR4H\_T13STR SET 0

; RMAP=0 PAGE=0 - CCU6 Timer Control 4 Register Low

CCU6\_TCTR4L\_DTRES SET 0

CCU6\_TCTR4L\_T12RES SET 0

CCU6\_TCTR4L\_T12RR SET 0

CCU6\_TCTR4L\_T12RS SET 0

CCU6\_TCTR4L\_T12STD SET 0

CCU6\_TCTR4L\_T12STR SET 0

; RMAP=0 PAGE=2 - CCU6 Trap Control Register High

CCU6\_TRPCTRH\_TRPEN SET 0

CCU6\_TRPCTRH\_TRPEN13 SET 0

CCU6\_TRPCTRH\_TRPPEN SET 0

; RMAP=0 PAGE=2 - CCU6 Trap Control Register Low

CCU6\_TRPCTRL\_TRPM0 SET 0

CCU6\_TRPCTRL\_TRPM1 SET 0

CCU6\_TRPCTRL\_TRPM2 SET 0

; RMAP=0 PAGE=1 - SCU Clock Control Register

CMCON\_CLKREL SET 0

; RMAP=x - CPU Data Pointer Register High

DPH\_DPH0 SET 0

DPH\_DPH1 SET 0

DPH\_DPH2 SET 0

DPH\_DPH3 SET 0

DPH\_DPH4 SET 0

DPH\_DPH5 SET 0

DPH\_DPH6 SET 0

DPH\_DPH7 SET 0

; RMAP=x - CPU Data Pointer Register Low

DPL\_DPL0 SET 0

DPL\_DPL1 SET 0

DPL\_DPL2 SET 0

DPL\_DPL3 SET 0

DPL\_DPL4 SET 0

DPL\_DPL5 SET 0

DPL\_DPL6 SET 0

DPL\_DPL7 SET 0

; RMAP=x - CPU Extended Operation Register

EO\_DPSEL0 SET 0

EO\_TRAP\_EN SET 0

; RMAP=0 PAGE=0 - SCU External Interrupt Control Register 0

EXICON0\_EXINT0 SET 0

EXICON0\_EXINT1 SET 0

EXICON0\_EXINT2 SET 0

EXICON0\_EXINT3 SET 0

; RMAP=0 PAGE=0 - SCU External Interrupt Control Register 1

EXICON1\_EXINT4 SET 0

EXICON1\_EXINT5 SET 0

EXICON1\_EXINT6 SET 0

; RMAP=0 PAGE=1 - SCU Flash Error Address Register High

FEAH\_ECCERRADDR[15:8] SET 0

; RMAP=0 PAGE=1 - SCU Flash Error Address Register Low

FEAL\_ECCERRADDR[7:0] SET 0

; RMAP=1 - OCDS Hardware Breakpoints Data Register

HWBPDR\_HWBPXX SET 0

; RMAP=1 - OCDS Hardware Breakpoints Select Register

HWBPSR\_BPSEL SET 0

HWBPSR\_BPSEL\_P SET 0

; RMAP=0 PAGE=1 - SCU Identity Register

ID\_PRODID SET 0

ID\_VERID SET 0

; RMAP=x - CPU Interrupt Enable 0 Register

IEN0\_EA SET 1

IEN0\_ES SET 0

IEN0\_ET0 SET 1

IEN0\_ET1 SET 0

IEN0\_ET2 SET 0

IEN0\_EX0 SET 0

IEN0\_EX1 SET 0

; RMAP=x - CPU Module Interrupt Enable 1 Register

IEN1\_EADC SET 0

IEN1\_ECCIP0 SET 0

IEN1\_ECCIP1 SET 0

IEN1\_ECCIP2 SET 0

IEN1\_ECCIP3 SET 0

IEN1\_ESSC SET 0

IEN1\_EX2 SET 0

IEN1\_EXM SET 0

; RMAP=x - CPU Interrupt Priority 1 Register

IP1\_PADC SET 0

IP1\_PCCIP0 SET 0

IP1\_PCCIP1 SET 0

IP1\_PCCIP2 SET 0

IP1\_PCCIP3 SET 0

IP1\_PSSC SET 0

IP1\_PX2 SET 0

IP1\_PXM SET 0

; RMAP=x - CPU Interrupt Priority 1 High Register

IPH1\_PADCH SET 0

IPH1\_PCCIP0H SET 0

IPH1\_PCCIP1H SET 0

IPH1\_PCCIP2H SET 0

IPH1\_PCCIP3H SET 0

IPH1\_PSSCH SET 0

IPH1\_PX2H SET 0

IPH1\_PXMH SET 0

; RMAP=x - CPU Interrupt Priority High Register

IPH\_PSH SET 0

IPH\_PT0H SET 0

IPH\_PT1H SET 0

IPH\_PT2H SET 0

IPH\_PX0H SET 0

IPH\_PX1H SET 0

; RMAP=x - CPU Interrupt Priority Register

IP\_PS SET 0

IP\_PT0 SET 0

IP\_PT1 SET 0

IP\_PT2 SET 0

IP\_PX0 SET 0

IP\_PX1 SET 0

; RMAP=0 PAGE=0 - SCU Interrupt Request Register 0

IRCON0\_EXINT0 SET 0

IRCON0\_EXINT1 SET 0

IRCON0\_EXINT2 SET 0

IRCON0\_EXINT3 SET 0

IRCON0\_EXINT4 SET 0

IRCON0\_EXINT5 SET 0

IRCON0\_EXINT6 SET 0

; RMAP=0 PAGE=0 - SCU Interrupt Request Register 1

IRCON1\_ADCSRC0 SET 0

IRCON1\_ADCSRC1 SET 0

IRCON1\_EIR SET 0

IRCON1\_RIR SET 0

IRCON1\_TIR SET 0

; RMAP=1 - OCDS BreakPoints Control Register

MMBPCR\_HWB0C SET 0

MMBPCR\_HWB1C SET 0

MMBPCR\_HWB2C SET 0

MMBPCR\_HWB3C SET 0

MMBPCR\_SWBC SET 0

; RMAP=1 - OCDS Monitor Mode Control 2 Register

MMCR2\_EXBC SET 0

MMCR2\_EXBC\_P SET 0

MMCR2\_JENA SET 0

MMCR2\_MBCON SET 0

MMCR2\_MBCON\_P SET 0

MMCR2\_MMEP SET 0

MMCR2\_MMEP\_P SET 0

MMCR2\_MMODE SET 0

; RMAP=1 - OCDS Monitor Mode Control Register

MMCR\_MEXIT SET 0

MMCR\_MEXIT\_P SET 0

MMCR\_MRAMS SET 0

MMCR\_MRAMS\_P SET 0

MMCR\_MSTEP SET 0

MMCR\_MSTEP\_P SET 0

MMCR\_RRF SET 0

MMCR\_TRF SET 0

; RMAP=1 - OCDS Monitor Mode Data Transfer Register Receive

MMDR\_MMRR SET 0

; RMAP=1 - OCDS Monitor Mode Interrupt Control Register

MMICR\_DRETR SET 0

MMICR\_DVECT SET 0

MMICR\_MMUIE SET 0

MMICR\_MMUIE\_P SET 0

MMICR\_RRIE SET 0

MMICR\_RRIE\_P SET 0

; RMAP=1 - OCDS Monitor Mode Status Register

MMSR\_EXBF SET 0

MMSR\_HWB0F SET 0

MMSR\_HWB1F SET 0

MMSR\_HWB2F SET 0

MMSR\_HWB3F SET 0

MMSR\_MBCAM SET 0

MMSR\_MBCIN SET 0

MMSR\_SWBF SET 0

; RMAP=0 PAGE=0 - SCU Peripheral Input Select Register

MODPISEL\_EXINT0IS SET 0

MODPISEL\_JTAGTCKS SET 0

MODPISEL\_JTAGTDIS SET 0

MODPISEL\_URRIS SET 0

; RMAP=0 PAGE=0 - SCU NMI Control Register

NMICON\_NMIECC SET 0

NMICON\_NMIFLASHTIMER SET 0

NMICON\_NMIOCDS SET 0

NMICON\_NMIPLL SET 0

NMICON\_NMIVDD SET 0

NMICON\_NMIVDDP SET 0

NMICON\_NMIWDT SET 0

; RMAP=0 PAGE=0 - SCU NMI Status Register

NMISR\_FNMIECC SET 0

NMISR\_FNMIFLASHTIMER SET 0

NMISR\_FNMIOCDS SET 0

NMISR\_FNMIPLL SET 0

NMISR\_FNMIVDD SET 0

NMISR\_FNMIVDDP SET 0

NMISR\_FNMIWDT SET 0

; RMAP=0 PAGE=1 - SCU OSC Control Register

OSC\_CON\_ORDRES SET 0

OSC\_CON\_OSCPD SET 0

OSC\_CON\_OSCR SET 0

OSC\_CON\_OSCSS SET 1

OSC\_CON\_XPD SET 1

; RMAP=0 PAGE=2 - PORT P0 Alternate Select 0 Register

P0\_ALTSEL0\_P0 SET 0

P0\_ALTSEL0\_P1 SET 0

P0\_ALTSEL0\_P2 SET 0

P0\_ALTSEL0\_P3 SET 0

P0\_ALTSEL0\_P4 SET 0

P0\_ALTSEL0\_P5 SET 0

; RMAP=0 PAGE=2 - PORT P0 Alternate Select 1 Register

P0\_ALTSEL1\_P0 SET 0

P0\_ALTSEL1\_P1 SET 0

P0\_ALTSEL1\_P2 SET 0

P0\_ALTSEL1\_P3 SET 0

P0\_ALTSEL1\_P4 SET 0

P0\_ALTSEL1\_P5 SET 0

; RMAP=0 PAGE=0 - PORT P0 Data Register

P0\_DATA\_P0 SET 0

P0\_DATA\_P1 SET 0

P0\_DATA\_P2 SET 0

P0\_DATA\_P3 SET 0

P0\_DATA\_P4 SET 0

P0\_DATA\_P5 SET 0

; RMAP=0 PAGE=0 - PORT P0 Direction Register

P0\_DIR\_P0 SET 0

P0\_DIR\_P1 SET 0

P0\_DIR\_P2 SET 0

P0\_DIR\_P3 SET 0

P0\_DIR\_P4 SET 0

P0\_DIR\_P5 SET 0

; RMAP=0 PAGE=3 - PORT P0 Open Drain Control Register

P0\_OD\_P0 SET 0

P0\_OD\_P1 SET 0

P0\_OD\_P2 SET 0

P0\_OD\_P3 SET 0

P0\_OD\_P4 SET 0

P0\_OD\_P5 SET 0

; RMAP=0 PAGE=1 - PORT P0 Pull-Up/Pull-Down Enable Register

P0\_PUDEN\_P0 SET 0

P0\_PUDEN\_P1 SET 0

P0\_PUDEN\_P2 SET 1

P0\_PUDEN\_P3 SET 0

P0\_PUDEN\_P4 SET 0

P0\_PUDEN\_P5 SET 0

; RMAP=0 PAGE=1 - PORT P0 Pull-Up/Pull-Down Select Register

P0\_PUDSEL\_P0 SET 1

P0\_PUDSEL\_P1 SET 1

P0\_PUDSEL\_P2 SET 1

P0\_PUDSEL\_P3 SET 1

P0\_PUDSEL\_P4 SET 1

P0\_PUDSEL\_P5 SET 1

; RMAP=0 PAGE=2 - PORT P1 Alternate Select 0 Register

P1\_ALTSEL0\_P0 SET 0

P1\_ALTSEL0\_P1 SET 0

P1\_ALTSEL0\_P5 SET 0

P1\_ALTSEL0\_P6 SET 0

P1\_ALTSEL0\_P7 SET 0

; RMAP=0 PAGE=2 - PORT P1 Alternate Select 1 Register

P1\_ALTSEL1\_P0 SET 0

P1\_ALTSEL1\_P1 SET 1

P1\_ALTSEL1\_P5 SET 0

P1\_ALTSEL1\_P6 SET 0

P1\_ALTSEL1\_P7 SET 0

; RMAP=0 PAGE=0 - PORT P1 Data Register

P1\_DATA\_P0 SET 0

P1\_DATA\_P1 SET 0

P1\_DATA\_P5 SET 0

P1\_DATA\_P6 SET 0

P1\_DATA\_P7 SET 0

; RMAP=0 PAGE=0 - PORT P1 Direction Register

P1\_DIR\_P0 SET 0

P1\_DIR\_P1 SET 1

P1\_DIR\_P5 SET 0

P1\_DIR\_P6 SET 0

P1\_DIR\_P7 SET 0

; RMAP=0 PAGE=3 - PORT P1 Open Drain Control Register

P1\_OD\_P0 SET 0

P1\_OD\_P1 SET 0

P1\_OD\_P5 SET 0

P1\_OD\_P6 SET 0

P1\_OD\_P7 SET 0

; RMAP=0 PAGE=1 - PORT P1 Pull-Up/Pull-Down Enable Register

P1\_PUDEN\_P0 SET 1

P1\_PUDEN\_P1 SET 1

P1\_PUDEN\_P5 SET 1

P1\_PUDEN\_P6 SET 1

P1\_PUDEN\_P7 SET 1

; RMAP=0 PAGE=1 - PORT P1 Pull-Up/Pull-Down Select Register

P1\_PUDSEL\_P0 SET 1

P1\_PUDSEL\_P1 SET 1

P1\_PUDSEL\_P5 SET 1

P1\_PUDSEL\_P6 SET 1

P1\_PUDSEL\_P7 SET 1

; RMAP=0 PAGE=0 - PORT P2 Data Register

P2\_DATA\_P0 SET 0

P2\_DATA\_P1 SET 0

P2\_DATA\_P2 SET 0

P2\_DATA\_P3 SET 0

P2\_DATA\_P4 SET 0

P2\_DATA\_P5 SET 0

P2\_DATA\_P6 SET 0

P2\_DATA\_P7 SET 0

; RMAP=0 PAGE=1 - PORT P2 Pull-Up/Pull-Down Enable Register

P2\_PUDEN\_P0 SET 0

P2\_PUDEN\_P1 SET 0

P2\_PUDEN\_P2 SET 0

P2\_PUDEN\_P3 SET 0

P2\_PUDEN\_P4 SET 0

P2\_PUDEN\_P5 SET 0

P2\_PUDEN\_P6 SET 0

P2\_PUDEN\_P7 SET 0

; RMAP=0 PAGE=1 - PORT P2 Pull-Up/Pull-Down Select Register

P2\_PUDSEL\_P0 SET 1

P2\_PUDSEL\_P1 SET 1

P2\_PUDSEL\_P2 SET 1

P2\_PUDSEL\_P3 SET 1

P2\_PUDSEL\_P4 SET 1

P2\_PUDSEL\_P5 SET 1

P2\_PUDSEL\_P6 SET 1

P2\_PUDSEL\_P7 SET 1

; RMAP=0 PAGE=2 - PORT P3 Alternate Select 0 Register

P3\_ALTSEL0\_P0 SET 0

P3\_ALTSEL0\_P1 SET 0

P3\_ALTSEL0\_P2 SET 0

P3\_ALTSEL0\_P3 SET 0

P3\_ALTSEL0\_P4 SET 0

P3\_ALTSEL0\_P5 SET 0

P3\_ALTSEL0\_P6 SET 0

P3\_ALTSEL0\_P7 SET 0

; RMAP=0 PAGE=2 - PORT P3 Alternate Select 1 Register

P3\_ALTSEL1\_P0 SET 0

P3\_ALTSEL1\_P1 SET 0

P3\_ALTSEL1\_P2 SET 0

P3\_ALTSEL1\_P3 SET 0

P3\_ALTSEL1\_P4 SET 0

P3\_ALTSEL1\_P5 SET 0

P3\_ALTSEL1\_P6 SET 0

P3\_ALTSEL1\_P7 SET 0

; RMAP=0 PAGE=0 - PORT P3 Data Register

P3\_DATA\_P0 SET 0

P3\_DATA\_P1 SET 0

P3\_DATA\_P2 SET 0

P3\_DATA\_P3 SET 0

P3\_DATA\_P4 SET 0

P3\_DATA\_P5 SET 0

P3\_DATA\_P6 SET 0

P3\_DATA\_P7 SET 0

; RMAP=0 PAGE=0 - PORT P3 Direction Register

P3\_DIR\_P0 SET 1

P3\_DIR\_P1 SET 1

P3\_DIR\_P2 SET 1

P3\_DIR\_P3 SET 1

P3\_DIR\_P4 SET 1

P3\_DIR\_P5 SET 1

P3\_DIR\_P6 SET 1

P3\_DIR\_P7 SET 1

; RMAP=0 PAGE=3 - PORT P3 Open Drain Control Register

P3\_OD\_P0 SET 0

P3\_OD\_P1 SET 0

P3\_OD\_P2 SET 0

P3\_OD\_P3 SET 0

P3\_OD\_P4 SET 0

P3\_OD\_P5 SET 0

P3\_OD\_P6 SET 0

P3\_OD\_P7 SET 0

; RMAP=0 PAGE=1 - PORT P3 Pull-Up/Pull-Down Enable Register

P3\_PUDEN\_P0 SET 0

P3\_PUDEN\_P1 SET 0

P3\_PUDEN\_P2 SET 0

P3\_PUDEN\_P3 SET 0

P3\_PUDEN\_P4 SET 0

P3\_PUDEN\_P5 SET 0

P3\_PUDEN\_P6 SET 1

P3\_PUDEN\_P7 SET 0

; RMAP=0 PAGE=1 - PORT P3 Pull-Up/Pull-Down Select Register

P3\_PUDSEL\_P0 SET 1

P3\_PUDSEL\_P1 SET 1

P3\_PUDSEL\_P2 SET 1

P3\_PUDSEL\_P3 SET 1

P3\_PUDSEL\_P4 SET 1

P3\_PUDSEL\_P5 SET 1

P3\_PUDSEL\_P6 SET 0

P3\_PUDSEL\_P7 SET 1

; RMAP=0 PAGE=1 - SCU Password Register

PASSWD\_MODE SET 0

PASSWD\_PASS SET 0

PASSWD\_PROTECT\_S SET 0

; RMAP=x - CPU Power Control Register

PCON\_GF0 SET 0

PCON\_GF1 SET 0

PCON\_IDLE SET 0

PCON\_SMOD SET 0

; RMAP=0 PAGE=1 - SCU PLL Control Register

PLL\_CON\_LOCK SET 0

PLL\_CON\_NDIV SET 11

PLL\_CON\_OSCDISC SET 0

PLL\_CON\_RESLD SET 0

PLL\_CON\_VCOBYP SET 0

; RMAP=0 PAGE=1 - SCU Power Mode Control Register 0

PMCON0\_PD SET 0

PMCON0\_SD SET 0

PMCON0\_WDTRST SET 0

PMCON0\_WKRS SET 0

PMCON0\_WKSEL SET 0

PMCON0\_WS SET 0

; RMAP=0 PAGE=1 - SCU Power Mode Control Register 1

PMCON1\_ADC\_DIS SET 0

PMCON1\_CCU\_DIS SET 0

PMCON1\_SSC\_DIS SET 0

PMCON1\_T2\_DIS SET 0

; RMAP=0 - PORT Page Register

PORT\_PAGE\_OP SET 0

PORT\_PAGE\_PAGE SET 0

PORT\_PAGE\_STNR SET 0

; RMAP=x - CPU Program Status Word Register

PSW\_AC SET 0

PSW\_CY SET 0

PSW\_F0 SET 0

PSW\_F1 SET 0

PSW\_OV SET 0

PSW\_P SET 0

PSW\_RS0 SET 0

PSW\_RS1 SET 0

; RMAP=x - CPU Serial Data Buffer Register

SBUF\_VAL SET 0

; RMAP=x - CPU Serial Channel Control Register

SCON\_RB8 SET 0

SCON\_REN SET 1

SCON\_RI SET 0

SCON\_SM0 SET 0

SCON\_SM1 SET 1

SCON\_SM2 SET 0

SCON\_TB8 SET 0

SCON\_TI SET 0

; RMAP=0 - SCU Page Register

SCU\_PAGE\_OP SET 0

SCU\_PAGE\_PAGE SET 0

SCU\_PAGE\_STNR SET 0

; RMAP=x - CPU Stack Pointer Register

SP\_SP SET 0

; RMAP=0 - SSC Baudrate Timer Reload Register High

SSC\_BRH\_BR\_VALUE[15:8] SET 0

; RMAP=0 - SSC Baudrate Timer Reload Register Low

SSC\_BRL\_BR\_VALUE[7:0] SET 0

; RMAP=0 - SSC Module Control Register High, Operating Mode

SSC\_CONH\_O\_BE SET 0

SSC\_CONH\_O\_BSY SET 0

SSC\_CONH\_O\_EN SET 0

SSC\_CONH\_O\_MS SET 0

SSC\_CONH\_O\_PE SET 0

SSC\_CONH\_O\_RE SET 0

SSC\_CONH\_O\_TE SET 0

; RMAP=0 - SSC Module Control Register High Programming Mode

SSC\_CONH\_P\_AREN SET 0

SSC\_CONH\_P\_BEN SET 0

SSC\_CONH\_P\_EN SET 0

SSC\_CONH\_P\_MS SET 0

SSC\_CONH\_P\_PEN SET 0

SSC\_CONH\_P\_REN SET 0

SSC\_CONH\_P\_TEN SET 0

; RMAP=0 - SSC Module Control Register Low, Operating Mode

SSC\_CONL\_O\_BC SET 0

; RMAP=0 - SSC Module Control Register Low Programming Mode

SSC\_CONL\_P\_BM SET 1

SSC\_CONL\_P\_HB SET 0

SSC\_CONL\_P\_LB SET 0

SSC\_CONL\_P\_PH SET 0

SSC\_CONL\_P\_PO SET 0

; RMAP=0 - SSC Port Input Select Register

SSC\_PISEL\_CIS SET 0

SSC\_PISEL\_MIS SET 0

SSC\_PISEL\_SIS SET 0

; RMAP=0 - SSC Receiver Buffer Register Low

SSC\_RBL\_RB\_VALUE SET 0

; RMAP=0 - SSC Transmitter Buffer Register Low

SSC\_TBL\_TB\_VALUE SET 0

; RMAP=x - SCU System Control Register 0

SYSCON0\_RMAP SET 0

; RMAP=0 - T2 Timer 2 Reload/Capture Register High

T2\_RC2H\_RC2[15:8] SET 0

; RMAP=0 - T2 Timer 2 Reload/Capture Register Low

T2\_RC2L\_RC2[7:0] SET 0

; RMAP=0 - T2 Timer 2 Control Register

T2\_T2CON\_CP\_RL2 SET 0

T2\_T2CON\_EXEN2 SET 0

T2\_T2CON\_EXF2 SET 0

T2\_T2CON\_TF2 SET 0

T2\_T2CON\_TR2 SET 0

; RMAP=0 - T2 Timer 2 Register High

T2\_T2H\_THL2[15:8] SET 0

; RMAP=0 - T2 Timer 2 Register Low

T2\_T2L\_THL2[7:0] SET 0

; RMAP=0 - T2 Timer 2 Mode Register

T2\_T2MOD\_DCEN SET 0

T2\_T2MOD\_EDGESEL SET 0

T2\_T2MOD\_PREN SET 0

T2\_T2MOD\_T2PRE SET 0

; RMAP=x - CPU Timer Control Register

TCON\_IE0 SET 0

TCON\_IE1 SET 0

TCON\_IT0 SET 0

TCON\_IT1 SET 0

TCON\_TF0 SET 0

TCON\_TF1 SET 0

TCON\_TR0 SET 1

TCON\_TR1 SET 0

; RMAP=x - CPU Timer 0 Register High

TH0\_VAL SET 0

; RMAP=x - CPU Timer 1 Register High

TH1\_VAL SET 0

; RMAP=x - CPU Timer 0 Register Low

TL0\_VAL SET 0

; RMAP=x - CPU Timer 1 Register Low

TL1\_VAL SET 0

; RMAP=x - CPU Timer Mode Register

TMOD\_GATE0 SET 0

TMOD\_GATE1 SET 0

TMOD\_T0M SET 2

TMOD\_T1M SET 0

; RMAP=1 - WDT Watchdog Timer Control Register

WDTCON\_WDTEN SET 0

WDTCON\_WDTIN SET 0

WDTCON\_WDTPR SET 0

WDTCON\_WDTRS SET 0

WDTCON\_WINBEN SET 0

; RMAP=1 - WDT Watchdog Timer Register High

WDTH\_WDT[15:8] SET 0

; RMAP=1 - WDT Watchdog Timer Register Low

WDTL\_WDT[7:0] SET 0

; RMAP=1 - WDT Watchdog Timer Reload Register

WDTREL\_WDTREL SET 0

; RMAP=1 - WDT Watchdog Window-Boundary Count Register

WDTWINB\_WDTWINB SET 0